METHOD AND APPARATUS FOR PREVENTION OF READ CORRUPTION
IN ROTATED-READ REGISTER FILES AND CONTENT ADDRESSABLE
MEMORY ARRAYS

Karthik Balakrishnan

FIELD OF THE INVENTION

The present invention relates generally to "Rotated Read" register file memory structures and "Content Addressable Memory" structures, and, more particularly, to a method and structure for preventing read corruption in "Rotated Read" register file memory structures and "Content Addressable Memory" structures.

15

20

25

30

40

5

10

BACKGROUND OF THE INVENTION

As the performance of microprocessors and processing systems has continued to advance, more and more systems have begun to incorporate memory structures other than standard register files that read and write data on a row-by row basis. Two examples of memory structures that are not standard register files are "Rotated-Read" register file memory structures and "Content Addressable Memory" (CAM) arrays. In both rotated-read register file memory structures and CAM arrays data is read a column at a time across a given row rather than on a strictly row-by-row basis.

Using the column reads associated with rotatedread register file memory structures and CAM arrays it is possible, and often happens, that a read operation of a given memory cell can take place at the same time the row containing the memory cell is being written to and before the given cell has been written to.

35 Consequently, two problems result.

The first problem that occurred when a column read operation took place at the same time a row was being written to was that the data read in this situation was incorrect or "bad" data. This "bad" data problem was easily corrected by methods and structures well known

to those of skill in the art whereby the "bad" data was ignored and the correct data was read on the next read Consequently, from an architectural standpoint the "bad" data problem was a non-issue and a nonproblem.

However, the second, and far more troublesome, problem that occurred when a column read operation took place at the same time a row was being written to was that the value being read was typically an unknown, or indeterminate, value that was neither a digital zero nor a digital one, i.e., the value read was between a digital low and a digital high. As noted above, from an architectural standpoint, this was a non-issue; the correct data was simply read on the next cycle. However, the indeterminate value read when a column read operation took place at the same time a row was being written to resulted in the indeterminate values being propagated down stream to the sensing elements, logic elements, or other downstream circuitry of the system and, since the indeterminate value was neither a digital low nor a digital high, the downstream circuitry often failed because the downstream circuits were designed to process signals consisting of either a digital low or a digital high but not an intermediate value. Consequently, the effects of the indeterminate 25 value that resulted a column read operation took place at the same time a row was being written to on downstream circuitry was often circuit failure and it was found that correcting this problem in silicon was extremely difficult.

10

20

30

What is needed is a method and apparatus for preventing read corruption in rotated-read register file memory structures and CAM array structures by preventing indeterminate, or intermediate, values from being propagated to sensing elements, logic circuits, or other circuitry downstream from the memory structure and ensuring that the sensing elements, logic circuits,

or other downstream circuitry receive only defined digital low or digital high signals.

SUMMARY OF THE INVENTION

10

15

20

25

30

35

The present invention is directed to a method and apparatus for preventing read corruption in rotated-read register file memory structures and CAM array structures by preventing indeterminate, or intermediate, values from being propagated to sensing elements, logic circuits, or other circuitry downstream from the memory structure and ensuring that the sensing elements, logic circuits, or other downstream circuitry receive only defined digital values.

According to the present invention, corruption prevention circuits are used to force a read bit line to a known digital value by discharging the read bit line when a cell structure is being written to at the same time a read is performed on the corresponding read word line. Consequently, according to the present invention, the value on the read bit line is forced to a known digital value by the corruption prevention circuit of the invention and the prior art problem of the value being read having an unknown or indeterminate value that is neither a digital low nor a digital high is eliminated. Therefore, using the method and structure of the invention, indeterminate values are never propagated down stream to the sensing elements, logic elements, or other downstream circuitry of the system and there is no potential failure of the downstream circuitry.

According to the present invention, corruption prevention circuits are specifically designed to be operatively coupled to the existing write word lines. Since write word lines are already required, there is minimal new structure added. In addition, the

corruption prevention circuits of the invention can be placed physically very close to read bit lines, in one embodiment on the order of five to ten microns from the edge of the array. This means that the addition of the corruption prevention circuits of the invention results in minimal additional capacitance and the size of the resulting improved rotated-read memory structure can be kept almost the same as prior art structures.

In addition, the transistors used in the corruption prevention circuits of the invention can be sized very small without adversely effecting the down stream timing, and, in some embodiments of the invention, the addition of corruption prevention circuits of the invention allows for additional delay times by either sizing the corruption prevention circuit components appropriately or by adding well known delay elements to the corruption prevention circuits of the invention.

It is to be understood that both the foregoing general description and following detailed description are intended only to exemplify and explain the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

25

30

35

10

15

20

The accompanying drawings, which are incorporated in, and constitute a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the advantages and principles of the invention. In the drawings:

FIG.1 is a simplified representation of a improved rotated-read memory structure, such as a rotated-read register file memory structure or CAM array, designed according to the principles of the present invention;

FIG.2 shows a more detailed representation of an exemplary portion of the improved rotated-read memory structure of FIG.1 including exemplary cell structures and an exemplary corruption prevention circuit designed according to the principles of the present invention;

FIG.3 shows a more detailed representation of an exemplary portion of the improved rotated-read memory structure of FIG.1 including exemplary cell structures and one embodiment of a corruption prevention circuit comprising a corruption prevention pull-down transistor designed according to the principles of the present invention; and

15 FIG.4 shows a more detailed representation of an exemplary portion of the improved rotated-read memory structure of FIG.1 including exemplary cell structures and another embodiment of a corruption prevention circuit comprising a corruption prevention pull-down transistor and a corruption prevention AND gate designed according to the principles of the present invention.

25 **DETAILED DESCRIPTION**

5

10

30

35

The invention will now be described in reference to the accompanying drawings. The same reference numbers may be used throughout the drawings and the following description to refer to the same or like parts.

The present invention is directed to a method and apparatus for preventing read corruption in rotated-read register file memory structures and CAM array structures (100 In FIG.1) by preventing indeterminate, or intermediate, values from being propagated to sensing elements, logic circuits, or other circuitry

downstream from the memory structure (161 in FIG.1) and ensuring that the sensing elements, logic circuits, or other downstream circuitry receive only defined digital values.

5

10

15

20

25

30

35

According to the present invention, corruption prevention circuits (105 in FIG.1, 127 in FIG.s 2, 3, and 4) are used to force a read bit line (141 in FIG.s 2, 3, and 4) to a known digital value by discharging the read bit line when a cell structure (121, 123 and 135 in FIG.s 2, 3, and 4) is being written to at the same time a read is performed on the corresponding read word line (101 in FIG.1 and 133, 135, and 137 in FIG.s 2, 3, and 4). Consequently, according to the present invention, the value on the read bit line is forced to a known digital value by the corruption prevention circuit and the prior art problem of the value being read having an unknown or indeterminate value that is neither a digital low nor a digital high is eliminated. Therefore, using the method and structure of the invention, indeterminate values are never propagated down stream to the sensing elements, logic elements, or other downstream circuitry of the system and there is no potential failure of the downstream circuitry.

According to the present invention, corruption prevention circuits are specifically designed to be operatively coupled to the existing write word lines 107 in FIG.1 and 151 in FIG.s 2, 3, and 4). Since write word lines are already required, there is, according to the invention, minimal new structure added. In addition, the corruption prevention circuits of the invention can be placed physically very close to read bit lines (141 in FIG.s 1, 2, 3, and 4), in one embodiment on the order of five to ten microns from the edge of the array. This means that the addition of the corruption prevention circuits of the invention results in minimal additional capacitance and the size of the

resulting improved rotated-read memory structure can be kept almost the same as prior art structures.

In addition, the transistors (301 in FIG.3 and 301 in FIG.5) used in the corruption prevention circuits of the invention can be sized very small without adversely effecting the down stream timing. In addition, in some embodiments of the invention, the addition of corruption prevention circuits of the invention allows for additional delay times by either sizing the corruption prevention circuit components (460 in FIG.4) appropriately or by adding well known delay elements (490 in FIG.4) to the corruption prevention circuits of the invention.

10

30

35

FIG.1 is a simplified representation of a improved 15 rotated-read memory structure 100, such as a rotatedread register file memory structure or CAM array, designed according to the principles of the present invention. As seen in FIG.1, improved rotated-read memory structure 100 includes: cell structures 104, 20 including exemplary cell structures 121, 123 and 125; read word lines 101, including exemplary read word lines 133, 135 and 137; read bit lines 103, including exemplary read bit line 141; write word lines 107, including exemplary write word line 151; and corruption 25 prevention circuits 105, including exemplary corruption prevention circuit 127.

As also shown in FIG.1, according to one embodiment of the present invention, each of write word lines 107 is operatively coupled to a corresponding one of corruption prevention circuits 105. As an example, exemplary write word line 151 is operatively coupled to exemplary corruption prevention circuit 127. In addition, as those of skill in the art will readily recognize, each of read bit lines 103 would be coupled to downstream circuitry such as the sensing elements, logic elements, or other downstream circuitry. As an example, exemplary read bit line 141 is shown

operatively coupled to exemplary downstream circuit 161.

As noted above, in one embodiment of the invention, improved rotated-read memory structure 100 is either a rotated-read register file memory structure or CAM array. In addition, in one embodiment of the invention, improved rotated-read memory structure 100 is comprised of full-swing single-ended read logic and is an "A" phase domino logic structure wherein the read and write operations take place in the same phase, i.e., the "A" phase. In addition those of skill in the art will readily recognize the size, i.e., the number of rows and columns of improved rotated-read memory structure 100 shown in FIG.1 was chosen arbitrarily for illustrative purposes only and that in practice the invention can be applied to any size memory.

10

15

20

25

30

35

As shown in FIG.1 and discussed above, according to the present invention improved rotated-read memory structure 100 includes a set of corruption prevention circuits 105 with each corruption prevention circuit 105 operatively coupled to a corresponding one of write word lines 107. According to the present invention, and as discussed in more detail with respect to FIG. 2, the purpose of corruption prevention circuits 105 is to force a known digital value onto a corresponding one of read bit lines 141 when a cell structure of a given row is being written to at the same time a read is performed. As also discussed below, according to the present invention, corruption prevention circuits 105 are specifically designed to be operatively coupled to the existing write word lines 107 since write word lines 107 are already employed. Consequently, according to the invention, there is minimal new structure added.

Those of skill in the art will recognize that while the corruption prevention circuits 105 of the invention are shown in FIG.1 as being operatively

coupled to the right side of improved rotated-read memory structure 100, corruption prevention circuits 105 could as easily be coupled to the left side of improved rotated-read memory structure 100 with minimal structural modification.

5

10

15

20

25

30

35

FIG.2 shows a more detailed representation of the exemplary portion 171 of improved rotated-read memory structure 100 of FIG.1 including exemplary cell structures 121, 123 and 125 and exemplary corruption prevention circuit 127. As seen in FIG.2, exemplary portion 171 of improved rotated-read memory structure 100 includes exemplary read word lines 133, 135 and In exemplary cell structure 121, exemplary read word line 133 is coupled to a first input 241 of NOR gate 203 and data cell 205 is coupled to second input 242 of NOR gate 203. An output 243 of NOR gate 203 is coupled to a gate 245 of pull down transistor 201. first flow electrode 246 of pull down transistor 201 is coupled to exemplary read bit line 141 and a second flow electrode 247 of pull down transistor 201 is coupled to a supply voltage 281.

Likewise, in exemplary cell structure 123, exemplary read word line 135 is coupled to a first input 251 of NOR gate 213 and data cell 215 is coupled to second input 252 of NOR gate 213. An output 253 of NOR gate 213 is coupled to a gate 254 of pull down transistor 211. A first flow electrode 256 of pull down transistor 211 is coupled to exemplary read bit line 141 and a second flow electrode 257 of pull down transistor 211 is coupled to supply voltage 281.

Likewise, in exemplary cell structure 125, exemplary read word line 137 is coupled to a first input 261 of NOR gate 223 and data cell 225 is coupled to second input 262 of NOR gate 223. An output 263 of NOR gate 223 is coupled to a gate 264 of pull down transistor 221. A first flow electrode 266 of pull down transistor 221 is coupled to exemplary read bit

line 141 and a second flow electrode 267 of pull down transistor 221 is coupled to supply voltage 281.

As also shown in FIG.2, portion 171 of improved rotated-read memory structure 100 includes write word line AND gate 260 with write word enable input 261 and clock signal input 262. In one embodiment, output 263 of AND gate 260 is operatively coupled to exemplary write word line 151 and a first terminal 227 of exemplary corruption prevention circuit 127. A second terminal 237 of exemplary corruption prevention circuit 127 is coupled to exemplary read bit line 141.

10

15

20

25

30

35

As discussed above, according to the present invention, exemplary corruption prevention circuit 127 is used to force a known digital value onto exemplary read bit line 141 when a cell structure, such as exemplary cell structures 121, 123 or 125, is being written to at the same time a read is performed on the corresponding read bit line 141. Consequently, according to the present invention, the value on exemplary read bit line 141 is forced to a digital low or a digital high by corruption prevention circuit 127 and the prior art problem of the value being read having an unknown or indeterminate value that is neither a digital zero nor a digital one is eliminated. Therefore, using the method and structure of the invention, indeterminate values are never propagated down stream to the sensing elements, logic elements, or other downstream circuitry of the system (not shown) and there is no potential failure of the downstream circuitry.

FIG.3, like FIG.2, shows a more detailed representation of the exemplary portion 171 of improved rotated-read memory structure 100 of FIG.1 including a specific embodiment of an exemplary corruption prevention circuit 127 that comprises a corruption prevention pull down transistor 301. As with FIG.2, FIG.3 shows exemplary cell structures 121, 123 and 125

and exemplary corruption prevention circuit 127. As seen in FIG.3, exemplary portion 171 of improved rotated-read memory structure 100 includes exemplary read word lines 133, 135 and 137. In exemplary cell structure 121, exemplary read word line 133 is coupled to a first input 241 of NOR gate 203 and data cell 205 is coupled to second input 242 of NOR gate 203. An output 243 of NOR gate 203 is coupled to a gate 245 of pull down transistor 201. A first flow electrode 246 of pull down transistor 201 is coupled to exemplary read bit line 141 and a second flow electrode 247 of pull down transistor 201 is coupled to supply voltage 281.

10

20

25

30

Likewise, in exemplary cell structure 123, exemplary read word line 135 is coupled to a first input 251 of NOR gate 213 and data cell 215 is coupled to second input 252 of NOR gate 213. An output 253 of NOR gate 213 is coupled to a gate 254 of pull down transistor 211. A first flow electrode 256 of pull down transistor 211 is coupled to exemplary read bit line 141 and a second flow electrode 257 of pull down transistor 211 is coupled to supply voltage 281.

Likewise, in exemplary cell structure 125, exemplary read word line 137 is coupled to a first input 261 of NOR gate 223 and data cell 225 is coupled to second input 262 of NOR gate 223. An output 263 of NOR gate 223 is coupled to a gate 264 of pull down transistor 221. A first flow electrode 266 of pull down transistor 221 is coupled to exemplary read bit line 141 and a second flow electrode 267 of pull down transistor 221 is coupled to supply voltage 281.

As also shown in FIG.3, portion 171 of improved rotated-read memory structure 100 includes write word line AND gate 260 with write word enable input 261 and clock signal input 262. Output 263 of AND gate 260 is operatively coupled to exemplary write word line 151. According to this embodiment of the invention, output

263 of AND gate 260 is also operatively down transists gate 305 of corruption prevention alectrode 303 of corruption electrode 303 of corruption alectrode 303 of corrupt gate 30° of corruption prevention 9011 down transion of corruption electrode 303 of corruption and a first flow prevention of corruption of corruption and a first flow prevention and a first flow pr and a first flow electrode 303 of corruption to ransistor 301 is coupled to prevention pull down transistor and a first read hit line in prevention pull down transistor second flow electrode is

prevention pull down transistor second franciator and is

prevention read bit line 141.

exemplary read nrevention null down transistor and is

exemplary read nrevention null down transistor and is exemplary read prevention pull down transistor 301 is

of corruption prevention 221 ed to supply voltage of the invention, exemplary in this embodiment In this embodiment of the invention, exemplar, and corruption circuit 127, and corruption prevention prevention transfer and is used to for a corruption and corruption prevention transistor 301, 141 hv discharging prevention pull down read hit line 141 hv discharging prevention pull onto read hit line 141 hv discharging prevention pull down transistor 301, is used to torce a auch of torce a such discharging pull down transistor line armormer and part of the prevention pull down transistor line armormer armormer and discharging armoration pull down transistor line armoration lin coupled to supply voltage 281. digital low value onto read bit line a cell structure, he included the line late of the la exemplary read pit line 141 when a cell structure, is being 123 or 125, is being 121, is nerformed on the same time a read is nerformed on the as exemplary cell structures a read is nerformed on the written to at the same as exemplary cell structures 121, 123 or 125, 15 pering on the written to at the same word line 133, 135 or 137. corresponding read word line 1331 in forced to a consequently according to the present in forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is forced to a consequently according to the present is a consequent to the consequent to the consequent to the present is a consequent to t Written to at the same time a read 18 performed 137.

Corresponding read word line to accompany the corresponding read word to the corresponding to the corr consequencly, according to the present invention, a consequencly, according to line line airmit of arminer of value on exemplary read plt line 141 is forced to a digital low by corruption prevention being and digital nation are rechief of the relief to the relief of digital low by corruption prevention the value being read having an the prior art problem of the value that is neither a the prior indererminate value. the prior art propiem of the value that is neither a unknown or indeterminate value that is neither a unknown or indeterminate value that is eliminated.

digital zero nor a digital one is eliminated. algical zero nor a digital one is eliminated. the method and structure of the method and structure of the method and structure or normalization indeterminate mains and normalization indeterminate in Theretore, indeterminate values are never propagated invention, invention of the general action of the general Invention, indeterminate values are never propagated or logic elements, including elements, including the sensing elements, averem (not shown) down stream to the circuitry of the averem other downstream circuitry of the other downstream circuitry of the sensing elements, averem (not shown) down stream to the sensing elements, logic elements, not shown)

other downstream circuitry failure of the downstream other there is no notential failure. other downstream potential failure of the downstream and there is no potential failure of the downstream As discussed above in the embodiment of the As alscussed above in the embodiment of the file invention shown in either a rotated real ster invention in is either a rotated real ster at ricture in in is either a rotated real ster invention in is either a rotated real stericture in invention in is either a rotated real stericture in invention in is either a rotated real stericture in invention in its either a rotated real stericture in its either a invention snown in Fig. 3 improved rotated register file a rotated register file structure 100 is either a rotated rotated rotated register. Structure improved ror ared-read memory in one in memory structure or CAM array. In addition, in one look and memory structure or CAM array. The addition and memory structure or came array. The addition and memory structure or came array. The addition and memory structure or came array. In one look and memory structure or came array. In one look and memory structure or came array. In one look array array. In one look array array. embodiment, improved rotated read memory structure low read logic and read logic are wherein the read is comprised of full-swing logic armsture wherein the read is comprised of full-swing logic armsture wherein the read lo is an "A" phase domino take nlace in the game nhase. circuitry. Is an "A" phase domino take place in the same phase, and write operations to addition the same and write operations to addition the same of avilled the same operations to addition the same of avilled the same phase, and write operations to addition the same phase of a village operations. and write operations take place in those of skill in addition, in addition, the aremniary nortion i.e., the aremniary recognize the aremniary marting i.e., will readily recognize the aremniary marting. the art will readily recognize the exemplary portion 35

171 of improved rotated-read memory structure 100 shows only a portion of one row of improved rotated-read memory structure 100. Consequently, as shown in FIG.1, according to the present invention, each row of improved rotated-read memory structure 100, would have a structure identical to FIG.3 at one of its ends. addition, as discussed above, the size, i.e., the number of rows and columns of improved rotated-read memory structure 100 shown in FIG.1 was chosen arbitrarily for illustrative purposes only and that in 10 practice the invention can be applied to any size memory. As also discussed above, those of skill in the art will recognize that while the exemplary corruption prevention circuit 127 of the invention is shown in 15 FIG.3 as being operatively coupled to the right side of improved rotated-read memory structure 100, corruption prevention circuits of the invention could as easily be coupled to the left side of improved rotated-read memory structure 100 with minimal structural modification. 20

As discussed above, according to the present invention, exemplary corruption prevention circuit 127, and corruption prevention pull down transistor 301, is specifically designed to be operatively coupled to the existing exemplary write word line 151. Since write word line 151 is already required, there is minimal new structure added. In addition, since, in the one embodiment shown in FIG.3, exemplary corruption prevention circuit 127 comprises corruption prevention pull down transistor 301, corruption prevention pull down transistor 301 can be placed physically very close to exemplary read bit line 141, in one embodiment a distance 231 is on the order of five to ten microns from the edge of the array. This means that the addition of exemplary corruption prevention circuit 127, and corruption prevention pull down transistor 301 results in minimal additional capacitance and the size

25

30

35

of the resulting improved rotated-read memory structure 100 can be kept almost the same as prior art structures. In addition, since the read word signal path along exemplary read word lines 133, 135 and 137 is much longer than the signal path from output 263 of write word AND gate 260 to gate 305 of corruption prevention pull down transistor 301, corruption prevention pull down transistor 301 can be sized very small without adversely effecting the down stream timing.

10

15

20

25

30

35

FIG.4, like FIG.2 and FIG.3, shows a more detailed representation of the exemplary portion 171 of improved rotated-read memory structure 100 of FIG.1 including a specific embodiment of an exemplary corruption prevention circuit 127 that comprises a corruption prevention pull down transistor 301, a corruption prevention AND gate 460 and a delay element 490. As with FIG.3, FIG.4 shows exemplary cell structures 121, 123 and 125 and exemplary corruption prevention circuit 127. As seen in FIG.4, exemplary portion 171 of improved rotated-read memory structure 100 includes exemplary read word lines 133, 135 and 137. In exemplary cell structure 121, exemplary read word line 133 is coupled to a first input 241 of NOR gate 203 and data cell 205 is coupled to second input 242 of NOR gate 203. An output 243 of NOR gate 203 is coupled to a gate 245 of pull down transistor 201. first flow electrode 246 of pull down transistor 201 is coupled to exemplary read bit line 141 and a second flow electrode 247 of pull down transistor 201 is coupled to supply voltage 281.

Likewise, in exemplary cell structure 123, exemplary read word line 135 is coupled to a first input 251 of NOR gate 213 and data cell 215 is coupled to second input 252 of NOR gate 213. An output 253 of NOR gate 213 is coupled to a gate 254 of pull down transistor 211. A first flow electrode 256 of pull

down transistor 211 is coupled to exemplary read bit down translator 211 18 coupled to exemplary read put down line 141 and a second flow electrode 257 of pull down line 141 and a second flow electrode 257 of pull down translator 211 is coupled to enroll, white of 201 is coupled to enroll, white of 201 is coupled to enroll. line 141 and a second riow electrone voltage 125.

transistor 211 is compled to supply retrieve 125. Likewise in exemplary cell structure 125. exemplary read word line 137 is coupled to a first exemplary read word line 131 18 coupled to a riret of NOR gate 223 and data cell 225 is coupled an outmit 261 of NOR gate 223 and data cell 201 an outmit 261 of NOR gate 201 of NOR gate 201 and the second input 261 of NOR gate 201 of NOR Input 261 of NOR gate 223 and data cell 225 is coupled input 262 of NOR gate 223. An output down to second input 262 of NOR gate 264 of mill down to second 223 is coupled and data cell 225 is coupled and da to second input 262 or NOR gate 223. An output 263

NOR gate 223 is coupled to a gate 264 of pull down

NOR gate 223 is reiror from a gate 264 of reiror NUX gate 223 18 coupled to a gate 264 of pull down
transistor 221. 221 is counted to a gate 264 of pull down
transistor 221. 221 is counted to a gate 264 of pull down
transistor 221. 221 is counted to a gate 264 of pull down
transistor 221. 221 is counted to a gate 264 of pull down
transistor 221. transistor 221. A first flow electrode 266 of pull transistor 221. 221 is coupled to exemplary read bit also transistor accord flow electrode 267 of mill down transistor accord flow electrode 268 of pull transition. down transistor 221 is coupled to exemplary read plt down line 141 and a second flow electrode 267 of pull down line 141 and a second flow electrode 267 of pull down transistor 221 is coupled to exemplary read plt pull down line 141 and a second flow electrode 267 of pull down line 141 and a second flow electrode 267 line 141 and a second riow electrode voltage 281.

transistor 221 is coupled to supply 171 of improve transistor 221 and in Err A BIBCOL 777 18 combined to subbit housings improved improved in EIG.4. Portion 111 of improved write more also shown in Etmoture in includes write more also also shown in Etmoture in includes write more also also shown in Etmoture in includes write more also also shown in Etmoture in includes write more also also shown in Etmoture in includes which includes which includes also shown in Etmoture in includes with the includes also shown in Etmoture in includes with the includes also shown in Etmoture in includes with the includes also shown in Etmoture in includes with the includes also shown in Etmoture in includes also shown in Etmoture in includes with the includes also shown in Etmoture in includes also shown in Etmoture in include i As also snown in Fig. 4, portion includes write word analy structure word enable innut 261 and rotated read memory write word enable innut 261 and rotated read memory with write word enable innut 261 and rotated and reate 260 with write word enable innut 261 and rotated read memory with write word enable innut 261 and rotated read memory with write word enable innut 261 and rotated read memory with write word enable innut 261 and rotated rota rotated-read memory structure word enable input 261 and or ate 260 with write word enable input 267 and or and other airmst 267 and or airmst 267 are 260 with write word enable input 267 are 260 with write word enable input 267 are 260 airmst 267 are 260 airmst 267 are line AND gate 260 with write word enable input 261 and output 263 of AND gate 161 output 263 of AND gate 161 clock signal input to exemplary write word line 161 clock signal counled to exemplary write word line 161 oneratively counled to clock signal input to exemplary write word line arahi
operatively coupled to exemplary write word arahi
operatively ambodiment of the invention operatively coupled to exemplary write word line able invention, write and is company of the invention, are sen is company to this embodiment of the invention, are sen is company to the invention, are sen is company to the invention. In this embodiment of the innut 461 of corruntion arevention input 261 of write word line and of corruntian arevention input and are word line are word enable input as write word enable to input as a write word enable to input a write word Input 261 or write word line 461 of corruption write word a write word signal input 269 of write word a write word and clock signal input 269 of write word a write word and clock signal input 269 of write word a write word and clock signal input 269 of write word a write word and clock signal input 269 of write word a write word and clock signal input 269 of write word a write word and clock signal input 269 of write word a write word and clock signal input 269 of write word a writ a write word enable input 461 or corruption prevention input 262 of write word input 262 of write and clock signal input 262 or airmal input 262 of write and clock signal input 262 of write and clock signal input 262 of write are along the armal input 262 of write are along the area are are along the armal area. ANU gate 400 and clock signal input to a clock signal input

line AND gate 260 is coupled to a create 100 AND core 100 AND gate 260 is correction and correc According to this embodiment of the invention AND gare 460.

According to this embodiment of the invention o The Ann gate 400 prevention AND gate 460. According to this embodiment of the invention and gate 460 is output 463 of corruption prevention of additional according to constant and the invention and output 463 or corruption prevention AND gate 460 18

output 463 or corruption input 491 of delay element
operatively and of delay alement and is one retired. operacively coupled to input 491 of delay element 40 peracively and output 493 of delay element 400 peracively elem and output 493 of delay element 490 18 operatively and output 493 of delay element 490 18 operation pull coupled to a gate 201 and a first flow of the coupled t coupled to a gate 301 and a first transistor and is down transistor are represented as a down transistor are represented to a gate 301 and a first transistor and is down transistor and transistor and transistor are represented to a gate 301 and a first transistor and transistor are represented to a gate 301 and a first transistor and transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first transistor are represented to a gate 302 and a first transistor are represented to a gate 302 and a first transistor and transistor are represented to a gate 302 and a first corruption prevention pull down translator 301 18 flow second flow prevention pull down line 141.

corruption prevention read bit line normal down coupled to exemplary read or coupled to exemplary read prevention or coupled to exemplary and of corruption or constant in the coupled to exemplary the coupled to exemplary or coupled to exemplary the coupled to exemplary the corruption of corruption or constant in the coupled to exemplary the coup coupled to exemplary read plt line 141. pull down electrode 307 of corruption prevention of corruption prevention are 201 electrode 301 of coupled to supply voltage around transistor 301 is coupled to the invention provided to the invention around transistor and around the transistory and the transit of the invention around the invention around the invention around the invention around the invention are the invention around the invention are the invention around the invention are the inven In this embodiment of the invention, and communication in this embodiment. In this embodiment of the invention, exemplars and corruption circuit 127, and corruption corruption are a corruption and corruption are a corruption are a corruption and corruption are a corruption are a corruption and corruption are a corruptio corruption prevention transistor 301 and corruption prevention pull down Prevention AND gate 460, are used to force a digital prevention AND gate 30

low value onto read bit line 141 when a cell structure, is heing exemplary read bit etructures 121. 122 or 125. is heing low value onto read bit line 141 by discharging exemplary read bit line lal when a cell structure, being lary read bit structures read is nerformed on the assex exemplary cell structures a read is nerformed on the assex exemplary the same time a read is nerformed on the written to at the same time. as exemplary cell structures 121, 123 or 123, 135 or 137.

Written to at read word line 133, 135 or 137. corresponding read word line last invention, the present invention, the present invention, the present invention, according to the present is forced to a corresponding according hir line last is forced to a corresponding according to the present is forced to a corresponding read hir line last is forced to a corresponding read word line last is forced to a corresponding read wor Corresponding read word line to the arrow. Consequently, according to the present invention, the value on exemplary read bit line at a constant of the value of exemplary read bit line at a constant of the value of exemplary read bit line at a constant of the value of exemplary read bit line at a constant of the value of value on exemplary read plt line lat is forced to a large on exemplary read plt line prevention circuit having digital low by corruption of the walve hairs read having digital prior art problem of the value hairs read having the prior art digital low by corruption prevention circuit 127 and having an digital low by problem of the value height art problem of the prior art indeterminate the prior indeterminate t the prior art proplem of the value being read have that is neither a unknown or indeterminate value that is neither a unknown or incereminate value that is eliminated.

digital zero nor a digital one is eliminated. digital zero nor a digital one is eliminated. the method and structure of roman and structure of the method and are never nroman indeterminate values are never nroman indeterminate. Therefore, indeterminate values are never propagated invention, invention, to the search of the sear invention, indeterminate values are never propagated or logic elements, invention, to the sensing elements, to the down stream circuitry of the down atream circuitry of the circuitry of the sensing elements, and the circuitry of the system (not shown) down stream to the sensing elements, failure of the downstream circultry failure of the downstream other there is no normatial failure. other downstream circuitry or the system (not snown)

other downstream potential failure of the downstream
and there is no potential As discussed above in the embodiment of the As discussed above in the embodiment of the invention in is airhar a rotated read register file Invention anown in rivial a rotated register file to addition in one structure are or cam array memory structure or CAM array. In addition, in one 100

In addition, in embodiment, improved rotated-read memory structure loo read logic and improved rotated-read memory read logic and wherein the read is comprised of full-swing single-ended wherein the read is comprised of homing logic arrunture wherein the read logic and homing logic arrunture wherein the read logic and logic and logic arrunture wherein the read logic and logic arrunture wherein the read logic 18 comprised of rull-swing single-ended read logic and wherein the read logic structure wherein the name nhage.

18 comprised of rull-swing single-ended wherein the game nhage.

18 an "A" phase domino have nlace in the game nhage. circuitry. 15 memory structure or CAM array. is an "A" phase domino take place in the same phase; and write operations to addition the same phase; i.e., the "A" phase. In addition, the exemplary portion and the exemplary portion and the exemplary recognize the exemplary at richire 100 and the art will readily rotated read memory at richire 100 and the art will readily rotated read memory at richire 100 and the art will readily recognize the exemplary portion shows the art will readily recognize the exemplary structure 100 shows are will readily recognize the exemplary portion of read memory at rotated read memory at rotated read memory at rotated read improved rotated row of improved row of impr only a portion of one row of improved rotated read only a portion of one row of improved rotated read only a portion of one row of improved rotated read only a portion on row of one row of the row o consequently! as shown in FIG.1! 20 the "A" phase. according to the present invention, each row ould have improved rotated read memory structure of its ende improved identical to ETC 4 at one of its ende memory scructure 100. consequently, as snown of each row of according to the present invention, at machine 100 improved rotated read memory structure of its ends.

improved rotated read to FIG.4 the sime is a structure identical to read the read r a structure identical to right the size rotated rotated above; improved rotated rotated addition; addition; and columns of improved rotated ro addition, as and columns of improved rotated read number of rows and columns of improved rotated read memory structure 100. memory structure illustrative purposes only and that arbitrarily for illustrative purposes number of tows and columns of improved rocated. I was chosen in FIG.1 was chosen memory structure 100 shown in FIG.1 was chosen. 35

practice the invention can be applied to any size memory. As also discussed above, those of skill in the art will recognize that while the exemplary corruption prevention circuit 127 of the invention is shown in FIG.4 as being operatively coupled to the right side of improved rotated-read memory structure 100, corruption prevention circuits of the invention could as easily be coupled to the left side of improved rotated-read memory structure 100 with minimal structural modification.

10

15

20

25

30

35

As discussed above, according to the present invention, exemplary corruption prevention circuit 127, and corruption prevention pull down transistor 301 and corruption prevention AND gate 460, is specifically designed to be operatively coupled to the existing exemplary write word line 151. Since write word line 151 is already required, there is minimal new structure In addition, since, in the one embodiment shown in FIG.4, exemplary corruption prevention circuit 127 comprises corruption prevention pull down transistor 301 and corruption prevention AND gate 460, corruption prevention pull down transistor 301 can be physically very close to exemplary read bit line 141, in one embodiment a distance 231 is on the order of five to ten microns from the edge of the array. This means that the addition of exemplary corruption prevention circuit 127, and corruption prevention pull down transistor 301 and corruption prevention AND gate 460, results in minimal additional capacitance and the size of the resulting improved rotated-read memory structure 100 can be kept almost the same as prior art structures.

In addition, since the read word signal path along exemplary read word lines 133, 135 and 137 is much longer than the signal path from output 463 of write word AND gate 460 to gate 305 of corruption prevention pull down transistor 301, corruption prevention pull

down transistor 301 can be sized very small without adversely errecting the addition, in this embodiment of the invention, addition of comment of addition of addition of comment of addition of comment of addition of comment of addition of adversely effecting the down of the down adversely effecting the down of the down of the down adversely effecting the down of addition of corruption prevention and his cirror addition additional delay, times if needed his cirror additional delay, the needed his cirror additional delay, and the needed his cirror additional delay, the needed his cirror additional delay, and the needed his cirror additional delay addit tor addition prevention AND gate 460 appropriately or by corruption prevention alements corruption prevention ANN gate 400 appropriately or by element

corruption prevention ANN elements, such as delay element

adding well know delay of corruption prevention and across a corruption adding the cutout across adding well know delay elements, such as delay elements and prevention and the output 463 of corruption prevention and 490, 100 the output 463 of corruption prevention and 490, 100 the output 463 of corruption prevention and 490, 100 the output 463 of corruption prevention and 490, 100 the output 463 of corruption prevention and 490, 100 the output 463 of corruption and 490 the output 46 AS gnown above, according to the present used to circuits are hy according to circuits are hy hy as gnown above, according to a known digital value hy invention, to a known digital value hy invention, aread hit line to a known digital value hy invention, aread hit line to a known digital value hy invention; corruption prevention circuits are used by line to a known digital value by force a read bit and r torce a read bit line to a known digital value by

torce a read bit line when a read is nerformed to be ind written to at the same time a read is nerformed. discharging the read pit line when a read is performed time a read is performed to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to at the same time a concernentive being written to a concerned to being written to at the same time a read 1s performed consequently!

being written to at the same time a read 1s performed the consequently!

being written to at the same time a read 1s performed the consequently! on the corresponding read word line. the value on the invention digital read to the present to a known digital read hit line is forced to according to the present invention, the value on the invention and the forced to a known the invention and the read bit line is forced in circuits of the invention of the invention circuits of the invention circuits of the invention circuits of the invention circuits of the invention and the corruntion prevention circuits of the invention of the invention circuits of the inventio gate 460. read bit line is torced to a known digital value by the invention and the corruption prevention of the value hairs read having an original art problem of the value hairs read having and the corruption prior art problem of the value hairs read having and the value hairs read having and the corruption and the value having and the value having and the corruption prior art problem of the value hairs read having and the value having and the corruption and the value having and the value having and the corruption of the value having and the value having and the value having and the corruption of the value having and the value having and the corruption prior are problem. corruption prevention circuits of the invention and for problem of the value being read having an prior art problem. 10 prior art problem or the value that is neither a unknown or indeterminate value that is neither a unknown or indeterminate value that is eliminated.

digital zero nor a digital one is eliminated. algital zero nor a algital one is eliminated. the of the method and structure of recognition are never property independent in Therefore, indeterminate values are never propagated to the sensing elements invention, invention to the sensing elements. Invention, indeterminate values are never propagated or logic elements, and there is down stream to the sensing elements, and there down stream circuitry of the down downstream circuitry of the other downstream circuitry of the downstream circuitry of th down stream to the sensing elements, logic elements, is down stream to the sensing of the system and there is other downstream circuitry of the downstream circuitry of th other downstream circultry of the downstream circultry of the potential failure of the no potential failure of the DEELLIAL LALLUTE OF THE GOOD ACCORDING TO THE DESENT invention, corruption prevention operatively coupled to are since write word lines are specifically designed to be since write word lines specifically designed lines. invention corruption prevention circuits are since write word lines are existing write word lines. Since write word lines added.

existing write word lines. Since write word lines added.

there is minimal new structure of the direction of the corruntion of the corruntion of the already required. The corruntion of the corruption of the already required, the corruption prevention rerverses to the the addition, he had now a cally rerverses to the invention of the corruption addition. In audicion the corrupcion prevention circuits of the invention can be placed physically very craer of fix invention can be in one embodiment on the order of invention lines. Invention can be placed physically very close to the rhis means in one embodiment on array.

The array in the edge of the array to ten microns from the edge of the array. existing write word lines. 25 This means to ten microns trom the edge of the array. the array. the edge of the array. the array. the edge of the array. This means do not the array. read by the edge of the array.

to ten microns from the edge of the array. of the invention results in minimal additional

capacitance and the size of the resulting improved capacitance and the structure can be kept almost the rotated read memory arrivariations In addition, the transistors used invention can be invention the transist of the invention the anum circuits of the affection the anum corruption prevention without adversally affecting the amall without adversally affecting the anall without adversally affect the anally without adversally and anally anally affects the anally adversally affect the anally and anally anally affects the anally and anally affects the anally and anally anally affects the anally and anally anally and anally anally affects the anally and anally and anally anally anally anally and anally anally anally anally anally anally anally and anally corruption prevention circuits of the down in addition in addition adversely effecting the down in addition in addition addition addition addition addition addition at reason to addition addition at reason to addition addition at reason and addition at reason at gized very small without adversely effecting the down in some embodiments of the In addition, in or corruntion prevention stream timing. same as Prior art structures. stream timing. In addition of corruption prevention invention the addition of corruption for addition of invention of the inv Invention of the invention corruption along for additional circuits of the airing the corruption of the invention the circuits of the sizing the corruption of the sizing the siz circuits of the sizing the corruption prevention times by either sizing the corruption or him adding the corruption or him adding the corruption of himself corrections. times by elther sizing the corruption prevention or by adding well circuit components appropriately or by adding circuit carcult components appropriately or by adding well known delay elements to the corruption prevention Its of the invention.

The foregoing description of an implementation of a implem the invention and description only invention to the illustration and incer not limit the invention and illustration and incer not limit the invention to the illustration and incer not limit the invention to the illustration and incer not limit the invention to the illustration and incer not limit the invention to the illustration and incer not limit the invention to the illustration and incer not limit the illustration and illustration and incer not limit the illustration and illustra the invention and description on an implementation the invention and description on an implementation and description only and therefore the invention and description only and the invention and description on an implementation of a i and therefore 18 and therefore 18 and therefore 18 invention to the invention and does not limit the invention and does not work from and does not work from and does not work from the exhaustive and the circuits of the invention. exhaustive and does not limit the invention to the Modifications and variations or many he are noseine in light of the arms teaching are noseine in light of Precise from nracticing the above teachings or may be are possible in nracticing the above teachings or may be are possible in nracticing the invention 10 Ired Irom practicing the invention. of skill in those instance, as noted above, the instance, as recommendation are instance, as recommendation. acquired from practicing the invention. the art will readily recognize improved retaining the art will readily recognize the size. the art will readily recognize the gize, i.e., the art will readily recognize improved rotated read number of rows and columns of row, in room, in memory structure 100 snown in Fig. 1 was cnosen that in arbitrarily for illustrative purposes only and size arbitrarily for invention can be applied to any size arbitrarily for livention can be applied to any gize practice the invention can be applied. In addition, those of skill in the art will circuits those of skill in the art will as being in FIG.1 as being recognize that while are shown in FIG.1 as being recognize invention are invention. 20 recognize that while the corruption prevention cil Tub or the invention are snown in Fight side of improved operatively coupled to the right someon, or making and operatively momon, or making the coupled to the right side of improved to rotated-read memory structure as easily be coupled to rotated-read memory in rotated-read memory improved rotated-read memory improved rotated-read memory it improved rotated read memory it is increased. operatively coupled to the right store of improvers to the right structure 100, corruption rotated read memory and the rotated read memory and prevention circuits 105 could as easily be coupled to structure improved rotated-read memory structure modification.

Prevention side of improved rotated-read modification at ructural modification. memory. In addition, was about in the Error for with minimal structural modification. other structures was shown in the FIG.s for 35

illustrative purposes only. Those of skill in the art will readily recognize that these specific structures could be readily exchanged, or modified, without departing from the scope and spirit of the present invention.

Consequently, the scope of the invention is defined by the claims and their equivalents.

10